PATENT APPLICATION
DOCKET NO.: 200300032-2

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Original) A system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

a first circuit portion for providing said data blocks including said header block to a second circuit portion;

control logic associated with said second circuit portion for processing said header block and generating, in response to said header block, a hint signal, wherein said hint signal is operable to be transferred via a synchronizer at least one data cycle prior to the transfer of said data blocks to a third circuit portion disposed in said second clock domain; and

a control block associated with said third circuit portion, said control block operating responsive to said hint signal to generate data transfer control signals for controlling said third circuit portion in order to control output of said data blocks in a particular ordered grouping.

2. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, further comprising a synchronizer controller disposed between said first and second clock domains for providing at least one dead cycle control signal to said second circuit portion, wherein said at least one dead cycle control signal is indicative of the location of at least one dead cycle between said first and second clock signal.

3. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said first circuit portion comprises a packet interface.

data blocks including a header block as recited in claim 1, wherein said second circuit portion comprises:

at least one queue operably coupled to said first circuit portion for temporarily storing said data blocks; and

a multiplexer (MUX) block operably coupled to said first circuit portion and said at least one queue, said MUX block operating under a MUX selection control signal generated by said control logic for selecting between data blocks stored in said at least one queue and data blocks provided by said first circuit portion without queuing, whereby said data blocks are transmitted as an output of said MUX block to said synchronizer.

5. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said third circuit portion comprises means for selecting between data blocks directly transmitted by said synchronizer and data blocks buffered in said second clock domain, said means operating responsive to at least a portion of said data transfer control signals.

6. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said header block provides protocol control information relative to said data blocks.

7. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein each of said data blocks comprises multiple bits.

8. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said data blocks include at least one interval interleaved therein.

9. (Original) The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said data blocks comprise multi-channeled packet data, each channel's data blocks being interleaved with data blocks of other channels.

10. (Original) A method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), comprising:

processing a header block associated with data blocks that are to be sent from said first clock domain to said second clock domain via a synchronizer;

generating a hint signal responsive to said header block and positioning said hint signal at least one cycle prior to the location of said data blocks;

transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain; and

generating appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

11. (Original) The method for effectuating the transfer of data blocks including a header block as recited in claim 10, further comprising:

generating advance notice indicative of the location of at least one dead cycle occurring between a first clock signal and a second clock signal used for transmitting data across a clock boundary;

receiving packet data and said advance notice indicative of the location of said at least one dead cycle;

calculating the optimal time to send said packet data relative to the location of said at least one dead cycle; and

transmitting ordered contiguous data blocks about said at least one dead cycle to a CLK1-to-CLK2 synchronizer for transmission to receive circuitry disposed in said second clock domain.

12. (Original) The method for effectuating the transfer of data blocks including a header block as recited in claim 11, wherein said at least one dead cycle comprises N - M dead cycles, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles such that N/M > 1.

13. (Original) A computer system having circuitry for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

means for processing a header block associated with said data blocks to determine said data blocks may be sent from said first clock domain to said second clock domain via a synchronizer;

means for generating a hint signal responsive to said header block wherein said hint signal is operable to be positioned at

least one cycle prior to the possible location of said data blocks; and

means for transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain, wherein said control block generates appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

14. (Original) The computer system as recited in claim 13, further comprising a multiplexer (MUX) block disposed in said second clock domain for operating responsive to at least a portion of said control signals.

15. (Original) The computer system as recited in claim 13, further comprising means for determining where a dead cycle occurs between said first and second clock signals.

16. (Original) The computer system as recited in claim 15, further comprising means for optimizing the position of said data blocks relative to said dead cycle.